LOW VOLTAGE RAIL-TO-RAIL CMOS OUTPUT STAGE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Patent Application No. 09/516,961 (Atty.

5 Docket No. 60178.300401) entitled Low Voltage Rail-to-Rail CMOS Output Stage, filed on 02/29/2000. This application is related to U.S. Patent Application No. 09/516,008 (Atty. Docket No. 60178.300301) entitled Low Voltage Rail-to-Rail CMOS Input Stage, filed on an even day herewith on behalf of Troy Stockstad, the disclosure of which is incorporated herein by reference.

10 BACKGROUND OF THE INVENTION

Operational amplifiers in current electronic devices are provided with an output stage for driving additional devices connected to the amplifier in a particular application. To be suitable for broad application, it is preferable to provide such output stages with various characteristics, such as a relatively large and symmetrical output swing, preferably rail-to-

15 rail. It is also desirable to have the output able to both source and sink a substantial amount of current in order to drive loads having a significant capacitive component. In addition, the output should dissipate a relatively low quiescent power to minimize power consumption when not driving such loads. Obviously, other characteristics such as stability, manufacturability, etc. are also important considerations.

20 Most prior art output stages capable of operating at one volt are push-pull class A output stages. In this case either the pull-up or the pull-down device is a current source, and the other device is configured in a common-source configuration. This results in a high level of power dissipation to drive large output loads.

To minimize power dissipation in the output stage, class AB stages are often used.

25 Such stages have relatively low quiescent power dissipation, yet are capable of driving large amounts of current.

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In bipolar technologies, low voltage push-pull output stages generally rely on controlling base current drive to the output transistors. Since bipolar transistors are current driven devices, the output current of the device can be controlled if the base is driven with a controlled current source. Since collector current is exponentially dependent upon the base-emitter voltage, a large change in output current can be realized for small changes in the base-emitter voltage. Thus, in a bipolar design capable of operating at one volt, a circuit may be designed to control the base current drive of the device, yet still achieve a high output current. However, in a CMOS circuit such techniques are not effective since the amount of output current is strictly a function of the amount of voltage between the gate and the source of the device (V_{GS}).

CMOS push-pull output stages are generally designed such that one transistor is driven directly from the input of the output stage, and a complimentary transistor is driven by an output network. However, conventional CMOS output networks are problematic in that a conventional CMOS output network may or may not drive the complimentary transistor hard enough to create a symmetrical output. This problem is further increased at low voltages, such as at one volt.

Prior art Figure 1 is a schematic diagram of a conventional CMOS output stage 100. The conventional output stage 100 includes P-channel transistor 102 and N-channel transistor 104 set in a push-pull configuration. In addition, output stage 100 includes P-channel transistor 106 and N-channel transistors 108, 110, and 112, as well as current source 114.

Conventional output stage 100 is an example of a IV CMOS push-pull output stage. Essentially, the drains of the P-channel transistor 102 and the N-channel transistor 104 are coupled together. In addition, the source of the P-channel transistor 102 is coupled to the positive power supply V_{CC}, while the source of the N-channel transistor 104 is coupled to the negative power supply V_{EE}. In this manner, the conventional output stage 100 achieves near rail-to-rail performance, until a load is placed at the output.

In order to provide negative drive capability, the conventional output stage 100 must be operated at a high quiescent current. Current source 114, along with the area ratios of NMOS transistors 108 and 104, set the maximum sink current capability of the output stage. The output sink current in NMOS 104 is controlled by replica PMOS transistor 106, which controls the bias to NMOS transistors 110 and 112. NMOS 110 then modulates the bias to

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output NMOS 104. The output drive capability of circuit 100 is not symmetrical, since the drain current in PMOS 102 is limited only by its V_{GS}, while the NMOS 104 can only deliver $I_{114} \cdot ((W/L_{104})/(W/L_{108}))$. This limits the type of applications that will function properly with output stage 100.

5　　　In view of the foregoing, what is needed is an output stage that provides near rail-to-rail performance, which does not require a high quiescent current to provide negative drive capability. Moreover, the output stage should be capable of operating from low supply voltages, such as slightly more than a single V_{GS} voltage.

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The present invention address this need by providing an output stage that provides essentially rail-to-rail performance, and operates from supply voltages down to slightly more than a single V_{GS} voltage. In one embodiment, an output stage suitable for low voltage operation and capable of providing an essentially symmetrical rail-to-rail output voltage is disclosed. The output stage includes a first field effect device having a first drain, a first gate, and a first source coupled to a power supply V_{CC}. The output stage further includes a second field effect device complimentary to the first field effect device, having a second drain, a second gate, and a second source coupled to a power supply having a nominal voltage of V_{EE}. Further, the second drain is coupled to the first drain. Also included in the output stage is an output sink network coupled to the second field effect device. The output sink network drives the second field effect device such that a product of a current in the first field effect device and a current in the second field effect device is essentially equal to a predetermined constant during operation of the output stage.

In another embodiment, a method for providing an output signal from an output stage of a low voltage amplifier capable of providing a substantially rail-to-rail output voltage is disclosed. The method comprises providing an input signal to a first field effect device having a first drain, a first gate, and a first source coupled to a power supply V_{CC}. Next, a second complimentary field effect device is driven utilizing an output sink network such that the product of the current in the first field effect device and the current in the second field effect device is essentially equal to a predetermined constant during operation of the amplifier.

In yet another embodiment, an application specific integrated circuit (ASIC) having an output stage for a low voltage operational amplifier is disclosed. The ASIC includes a first field effect device having a first drain, a first gate, and a first source coupled to a power supply V_{CC}. The ASIC further includes a second field effect device complimentary to the first field effect device, having a second drain, a second gate, and a second source coupled to a power supply having a nominal voltage of V_{EE}. Further, the second drain is coupled to the first drain. Also included in the ASIC is an output sink network coupled to the second field effect device. The output sink network drives the second field effect device such that the product of the current in the first field effect device and the current in the second field effect device is essentially equal to a predetermined constant during operation of the output stage.

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An operational amplifier output stage is disclosed in a further embodiment of the present invention. The operational amplifier output stage includes a push-pull output network that receives a first input signal and a second input signal, the first input signal being provided by an input signal V_{IN}. Also included in the operational amplifier output stage is an

5   output sink network that provides the second input signal to the push-pull output network.

Finally, an operational amplifier suitable for operating on low input voltage and capable of providing a substantially symmetrical rail-to-rail output voltage is disclosed. The operational amplifier includes an input stage and an output stage coupled to the input stage. Further, the output stage includes an output sink network.

10   Advantageously, the present invention provides essentially rail-to-rail performance, and does not require a high quiescent current to provide negative drive capability. Furthermore, the output stage of the present invention is capable of operating from a low supply voltage of slightly more than a single V_{GS} voltage.

The invention, together with further advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

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Prior Art Figure 1 is a schematic diagram of a conventional output stage;

Figure 2 is a block diagram showing an operational amplifier, in accordance with one embodiment of the present invention;

Figure 3 is a block diagram of an output stage, in accordance with an embodiment of the present invention;

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Figure 4 is a schematic diagram of an output stage, in accordance with one aspect of the present invention; and

Figure 5 is a schematic diagram of an output stage in accordance with another aspect of the present invention.

An invention is disclosed for providing an output stage that achieves essentially symmetrical rail-to-rail performance, and can operate with a voltage supply of slightly more than a single V_{GS} voltage. In the following description, numerous specific details are set

5 forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to those skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order not to unnecessarily obscure the present invention.

Figure 1 was described in terms of the prior art. Figure 2 is a block diagram showing

10 an operational amplifier 200, in accordance with one embodiment of the present invention. The operational amplifier 200 includes an input stage 202 and an output stage 204.

In operation, the input stage 202 receives a differential input signal V_{IN}. The input stage 202 then converts the differential input signal into a single output stage input signal, and then supplies the output stage input signal to the output stage 204. The output stage 204

15 receives the output stage input signal and converts it to an amplified output voltage V_O.

The output stage 204 provides essentially rail-to-rail performance, and is capable of operating with a voltage supply as low as essentially a single V_{GS} voltage. As described in greater detail subsequently, the output stage 204 utilizes an output sink network to achieve this functionality.

20 Figure 3 is a block diagram of an output stage 204, in accordance with an embodiment of the present invention. The output stage 204 includes a push-pull output 300 and output sink network 302. In use, the push-pull output 300 receives two input signals. One signal is received from the source V_{IN}, the other signal is received from the output sink network 302.

As shown in Figure 3, one side of the push-pull output 300 is driven directly by the

25 source signal V_{IN}, while the other side is controlled by the output sink network 302. The result is an output stage 204 that provides a symmetrical rail-to-rail output when driven at one volt.

Referring next to Figure 4, an output stage 400 is shown, in accordance with one embodiment of the present invention. The output stage 400 includes an output sink network

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302, and a push-pull output 300 having a P-channel transistor 402 and an N-channel transistor 404. The source of the P-channel transistor 402 is coupled to V_{CC}, while the source of the N-channel transistor 404 is coupled to V_{EE}. Finally, the drain of both the P-channel transistor 402 and the N-channel transistor 404 are coupled together.

5   In use, the P-channel transistor 402 is driven directly by the source voltage V_{IN}, while the N-channel transistor 404 is driven by the output sink network 302. To provide a push-pull output, the current in the P-channel transistor 402 and the N-channel transistor 404 are always equal to a constant when multiplied together.

        Thus, the present invention drives the P-channel transistor 402 directly with the
10   source voltage V_{IN}, and uses the output sink network to drive the N-channel transistor such that the product of the current in the P-channel transistor 402 and the N-channel transistor 404 is always equal to a predetermined constant. In other words, when the current in the P-channel transistor 402 is increased, the current in the N-channel transistor 404 is decreased, and vice-versa. It will be apparent to those skilled in the art that a similar approach is to
15   connect voltage V_{IN} to the gate of NMOS transistor 404, and have an output source network drive PMOS 402.

        Figure 5 is a schematic diagram of an output stage 500, in accordance with one aspect of the present invention. The output stage 500 includes a push-pull output 300 having P-channel transistor 402 and N-channel transistor 404, an output sink network 302, and P-
20   channel transistors 502, 504, and 506.

        The P-channel transistor 402 is configured in a common source configuration. P-channel transistor 502 is configured to replicate P-channel transistor 402 in order to track the current in transistor 402 at a predetermined ratio, such as 6:1. Thus, there is six times as much current in P-channel transistor 402 as there is in P-channel transistor 502. This current
25   is then sent to the output sink network 302 to provide the above mentioned constant current product of transistors 402 and 404, as described in greater detail subsequently.

        The output sink network 302 includes a loop of V_{GS} voltages. Beginning on the left side of Figure 5, N-channel transistor 508 is coupled in a diode connection providing one V_{GS}, and diode 510 provides a diode change to node n6. Both N-channel transistor 508 and
30   diode 510 have a current I. Thus, node n6 is essentially a bias node having one V_{GS} and one diode drop. Then from the gate of N-channel transistor 512 at node n6 to its source there is a

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one V_{GS} drop. N-channel transistor 514 provides one V_{GS} up from its source to its gate to node n13. Then back down one diode drop from diode 516. Finally, N-channel transistor 404 provides one V_{GS} drop.

Thus, going through the loop of V_{GS} voltages, there is the V_{GS} for N-channel transistor 508, plus the diode drop of diode 510, minus a V_{GS} of P-channel transistor 402, plus the V_{GS} of N-channel transistor 514, minus the diode drop of diode 516, minus the V_{GS} of N-channel transistor 404, all of which is equal to zero as set forth in the following equations:

(1) $(I_{P/3} - I)/(W/L_{512}) = I_{D512}$

(2) $I_D = I_{D0}(W/L)\exp(V_{gs}/nV_T)\exp(-V_S/V_T)-\exp(-V_d/V_T)$

(3) $nV_T\ln(I/(I_{D0}(W/L_{508})) + V_T\ln(I/I_S) - nV_T\ln((I_{P/3} - I)/(I_{D0}(W/L_{512}))) + nV_T\ln(2I/(I_{D0}(W/L_{514}))) - V_T\ln(2I/2I_S) - nV_T\ln(I_N/(I_{D0}(W/L_{404}))) = 0$

(4) $2I^2/((W/L_{508})(W/L_{514})) = ((I_{P/3} - I)(I_N))/((W/L_{512})(W/L_{404}))$

    K_1 $((I_P)(I_N))/(K_2)$ --> push-pull action

For quiescent point, $I_P = I_N = I_Q$

The above equations assume all MOSFETS operate in the sub threshold region. To calculate the quiescent current I_Q the following equation can be used:

(5) $(2I^2)/((W/L_{508})(W/L_{514})) = ((1/3)(I_Q^2) - (I_Q)(I))/ ((W/L_{512})(W/L_{404}))$

--> $(1/3)(I_Q^2) - (I_Q)(I) - (2I^2)(((W/L_{512})(W/L_{404}))/ ((W/L_{508})(W/L_{514}))) = 0$, which can be solved using the quadratic equation.

Similar equations can be derived for the MOSFETS operating in saturation. Essentially, in saturation:

(1) $I_N + I_P = K$,

wherein K is a constant value.

As can be seen in the above equations, diodes 510 and 516 cancel each other out. Their primary purpose is to create a voltage at the source of N-channel transistors 512 and 514 at node n10, which creates a current so the current sources can operate. In an alternate embodiment, diodes 510 and 516 mat be replaced by resistors, which perform essentially the same function.

Referring to equation (3) above, two times I^2, which is set by N-channel transistors 506 and 504, divided by the size of N-channel transistors 508 and 514 is equal to I_P, which is the current in P-channel transistor 402, multiplied by I_N, which is the current in N-channel transistor 404, divided by three, which is derived from the ratio of transistors 402 and 502 and 520 and 522, times the size of transistors 402 and 404. Thus, a symmetrical rail-to-rail push-pull output is achieved.

In use, output stage 500 is connected to the output of the input stage, as shown in Figure 2, and the P-channel devices are controlled directly. The output sink network 302 determines how to bias output P-channel transistor 402 such that a push-pull output is achieved.

In the present invention, there is no more than one V_{GS} and two V_{Dsat} from either rail. Thus, the present invention will operate at less than one volt.

In addition, unlike conventional output stages, the present invention is able to drive the gate voltage of N-channel transistor 404 to nearly V_{CC}. For example, if transistor 402 is turned off, so the gate voltage of transistor 402 is close to V_{CC}, the current in transistor 502 is reduced. But, transistor 504 is biased at 2I, while transistor 518 is biased at I. Thus, the voltage at the gate of transistor 404 will increase to within a saturation voltage of transistor 504 and the diode drop of diode 516. Thus, when the output is to be driven very hard, where the amplifier is open loop (i.e. the differential input voltage is large), the voltage at the gate of transistor 404 will increase dramatically, thus providing a very good output drive.

It should again be noted that although output stage 500 has been described with an output sink network to control NMOS 404, an alternative approach is to use an output source network similar to circuit 302 to drive PMOS 402, and drive NMOS 404 directly from input V_{IN}.

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While the present invention has been described in terms of several preferred embodiments, there are many alterations, permutations, and equivalents which may fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is: